

Precision, High Speed, JFET Input Operational Amplifier

DESCRIPTION

The RH1056A JFET input operational amplifiers combine precision specifications with high speed performance.

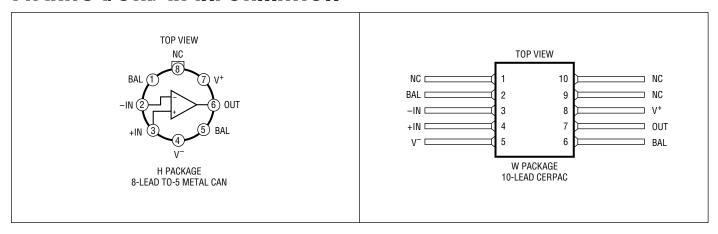
For the first time, $16V/\mu s$ slew rate and 6.5MHz gainbandwidth product are simultaneously achieved with offset voltage of typically $50\mu V$, $1.2\mu V/^{\circ}C$ drift, bias currents of 40pA at $70^{\circ}C$.

The wafer lots are processed to LTC's in-house Class S flow to yield circuits usable in stringent military applications.

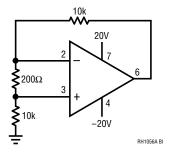
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±20V
Differential Input Voltage	±40V
Input Voltage	±20V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	-55°C to 125°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION



BURN-IN CIRCUIT





TOTAL DOSE BIAS CIRCUIT

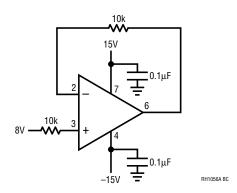


TABLE 1: ELECTRICAL CHARACTERISTICS (Preirradiation) (Note 2)

				T _A = 25°C			SUB-	$-55^{\circ}C \le T_A \le 125^{\circ}C$			SUB-	
SYMBOL	PARAMETER	CONDITIONS	NOTES	MIN	TYP	MAX	GROUP	MIN	TYP	MAX	GROUP	UNITS
V _{OS}	Input Offset Voltage		1			300	4			700	2, 3	μV
I _{OS}	Input Offset Current	Fully Warmed Up T _A = 125°C	3			10	1			1.5	2	pA nA
I _B	Input Bias Current	Fully Warmed Up T _A = 125°C	3			50	1			3.0	2	pA nA
R _{IN}	Input Resistance				10 ¹²							Ω
A _{VOL}	Large-Signal Voltage Gain	$V_S = \pm 15V, V_0 = \pm 10V, R_L = 2k$ $V_S = \pm 15V, V_0 = \pm 10V, R_L = 1k$		150 130			4 4	40			5,6	V/mV V/mV
$\overline{V_0}$	Output Voltage Swing	$V_S = \pm 15V, R_L = 2k$		±12			4	±12			5,6	V
V _{CM}	Input Common Mode Voltage Range	V _S = ±15V		±11			1	±11			2,3	V
CMRR	Common Mode Rejection Ratio	V _{CM} = ±11V V _{CM} = ±10.5V		86			1	85			2,3	dB dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V \text{ to } \pm 18V$ $V_S = \pm 10V \text{ to } \pm 17V$		90			1	88			2,3	dB dB
Is	Supply Current	V _S = ±15V				6.5	1					mA
SR	Slew Rate	$A_V = 1, V_S = \pm 15V$		12			7					V/µs
GBW	Gain-Bandwidth Product	V _S = ±15V			6.5							MHz
e _n	Input Noise Voltage Density	$V_S = \pm 15V$, f = 10Hz $V_S = \pm 15V$, f = 1kHz			28 14							nV/√Hz nV/√Hz
i _n	Input Noise Current Density	$V_S = \pm 15V$, f = 10Hz $V_S = \pm 15V$, f = 1kHz			1.8 1.8							fA/√Hz fA/√Hz
C _{IN}	Input Capacitance				4				4			pF

TABLE 1A: ELECTRICAL CHARACTERISTICS (Postirradiation) (Note 4)

OVMDOL	DADAMETED	CONDITIONS	NOTES	10KRAD(Si)		25KRAD(Si)		50KRAD(Si)		100KRAD(Si)		200KRAD(Si)		шите	
SYMBOL	PARAMETER	CONDITIONS	NOTES	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	
V_{0S}	Input Offset Voltage		1		300		300		370		570		570	μV	
I_{0S}	Input Offset Current		3		±10		±50		±150		±250		± 350	pA	
I _B	Input Bias Current		3		±50		±250		±500		±1000		±2000	pA	
A _{VOL}	Large-Signal Voltage Gain	$V_0 = \pm 10V, R_L \ge 2k$ $V_0 = \pm 10V, R_L \ge 1k$		150 130		150 130		150 130		100 87		75 65		V/mV V/mV	
$\overline{V_0}$	Output Voltage Swing			±12		±12		±12		±12		±12		V	
V _{CM}	Input Common Mode Voltage Range	V _S = ±15V		±11		±11		±11		±11		±11		V	
CMRR	Common Mode Rejection Ratio	V _{CM} = ±11V		86		86		86		86		86		dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V \text{ to } \pm 18V$		90		90		90		90		90		dB	
Is	Supply Current				7		7		7		7		7	mA	
SR	Slew Rate	$A_V = 1, V_S = \pm 15V$		12		12		12		12		12		V/µs	
C _{IN}	Input Capacitance			3(ур)	3((Тур)	3	(Typ)	3	(Тур)	3((Тур)	pF	

Note 1: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage. Offset voltage is measured under two different conditions: (a) approximately 0.5 seconds after application of power, (b) at $T_A = 25^{\circ}\text{C}$ only, with the chip heated to approximately 45°C to account for chip temperature rise when the device is fully warmed up.

Note 2: Unless otherwise stated, $V_S = \pm 15V$; and V_{OS} , I_B and I_{OS} are measured at $V_{CM} = 0V$.

Note 3: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J . Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D . $T_J = T_A + (\theta_{JA} \bullet P_D)$ where θ_{JA} is the thermal resistance from junction to ambient.

Note 4: Unless otherwise stated, $V_S = \pm 15 V$, $V_{CM} = 0 V$ and $T_A = 25 ^{\circ} C$.

TABLE 2: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP			
Final Electrical Test Requirements (Method 5004)	1*,2,3,4,5,6,7			
Group A Test Requirements (Method 5005)	1,2,3,4,5,6,7			
Group B and D for Class S, and Class C and D for Class B	1			
End Point Electrical Parameters (Method 5005)				

^{*} PDA applies to subgroup 1. See PDA Test Notes.

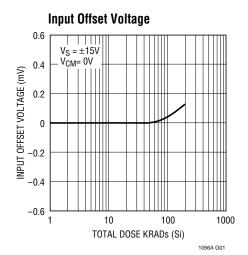
PDA Test Notes

The PDA is specified as 5% based on failures from group A, subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883. The verified failures of group A, subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.

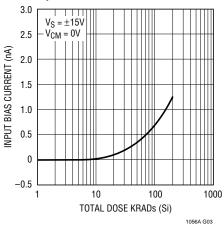
Linear Technology Corporation reserves the right to test to tighter limits than those given.



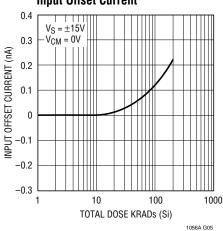
TYPICAL PERFORMANCE CHARACTERISTICS



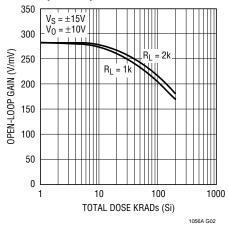
Input Bias Current 3.0



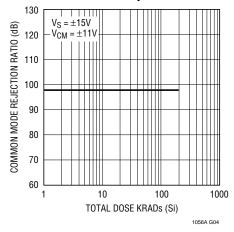
Input Offset Current



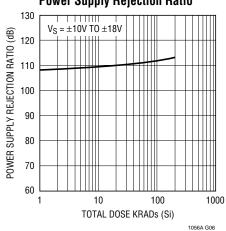
Open-Loop Gain



Common Mode Rejection Ratio



Power Supply Rejection Ratio



I.D. No. 66-10-0160 Rev. A 0698

